

## STRUCTURE AT A GLANCE

C P U	<b>Part 1:</b> Background and Motivation	<ul style="list-style-type: none"> <li>1. Combinational Digital Circuits</li> <li>2. Digital Circuits with Memory</li> <li>3. Computer System Technology</li> <li>4. Computer Performance</li> </ul>
	<b>Part 2:</b> Instruction-Set Architecture	<ul style="list-style-type: none"> <li>5. Instructions and Addressing</li> <li>6. Procedures and Data</li> <li>7. Assembly Language Programs</li> <li>8. Instruction-Set Variations</li> </ul>
	<b>Part 3:</b> The Arithmetic/Logic Unit	<ul style="list-style-type: none"> <li>9. Number Representation</li> <li>10. Adders and Simple ALUs</li> <li>11. Multipliers and Dividers</li> <li>12. Floating-Point Arithmetic</li> </ul>
	<b>Part 4:</b> Data Path and Control	<ul style="list-style-type: none"> <li>13. Instruction Execution Steps</li> <li>14. Control Unit Synthesis</li> <li>15. Pipelined Data Paths</li> <li>16. Pipeline Performance Limits</li> </ul>
	<b>Part 5:</b> Memory System Design	<ul style="list-style-type: none"> <li>17. Main Memory Concepts</li> <li>18. Cache Memory Organization</li> <li>19. Mass Memory Concepts</li> <li>20. Virtual Memory and Paging</li> </ul>
	<b>Part 6:</b> Input/Output and Interfacing	<ul style="list-style-type: none"> <li>21. Input/Output Devices</li> <li>22. Input/Output Programming</li> <li>23. Buses, Links, and Interfacing</li> <li>24. Context Switching and Interrupts</li> </ul>
	<b>Part 7:</b> Advanced Architectures	<ul style="list-style-type: none"> <li>25. Road to Higher Performance</li> <li>26. Vector and Array Processing</li> <li>27. Shared-Memory Multiprocessing</li> <li>28. Distributed Multicomputing</li> </ul>



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our.very.log.coding.and.then.we.start.to.transistors.so.that.was.computing.then.have...particles  
...and...they...bounce...around....design..space..is..relatively..flat..there's...you...sing...in...the...class..  
.and...you're...saying....natively...so...how...does...this...survive...on....instruction..set..architecture..a.  
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